

GOVERNMENT OF THE DISTRICT OF COLUMBIA
BOARD OF ZONING ADJUSTMENT



NOTICE OF VIRTUAL PUBLIC HEARING

TIME AND PLACE: Wednesday, April 23, 2025, @ 9:30 a.m.

Via WebEx: <https://dcoz.dc.gov/BZA04-23-2025>

Via Telephone: 202-860-2110 **Access code:** 2311 691 1915

Via YouTube: <https://www.youtube.com/c/DCOfficeofZoning>

Instructions: <https://dcoz.dc.gov/release/virtual-public-hearings>

Witness Sign Up: <https://dcoz.dc.gov/service/sign-testify>

**TO CONSIDER THE FOLLOWING APPLICATION THAT HAS BEEN ACCEPTED BY
THE OFFICE OF ZONING AND SCHEDULED FOR PUBLIC HEARING:**

Application No. 21273 of Livingston Developers Group, LLC

Address: 4184, 4190, and 4196 Livingston Road S.E. (Square 6219, Lots 22, 23, and 24)

ANC: 8D

Relief: Special Exception under:

- The new residential development standards of Subtitle U § 421 (pursuant to Subtitle X § 901.2)

Project: To construct nine additional dwelling units and a three-story rear addition with cellar on each lot, to three separate, three-story with cellar, 13-unit apartment houses in the RA-1 Zone.

This public hearing will be conducted in accordance with the contested case provisions of Subtitle Y, Chapters 4 & 5.

PLEASE NOTE:

The hearing date shown above may be RESCHEDULED prior to this date, in which case the new hearing date will be posted on the online calendar for the Board of Zoning Adjustment (“**Board**” or “**BZA**”), on the website of the Office of Zoning (“**OZ**”) at <https://dcoz.dc.gov/BZACalendar>, as well as on the case record webpage available on the Interactive Zoning Information System (“**IZIS**”) on the OZ website <https://dcoz.dc.gov/CaseRecord> (additional instructions below). **Please check these webpages to confirm the final hearing date and time** as there will be no other notice of these changes provided. One day before the hearing, the order of cases, agenda, and any other scheduling changes will be posted to the Board’s online calendar on OZ’s website.

Those who wish to testify at the public hearing **must** be present when their case is called. The order of cases may change at the Board’s discretion. Participants are encouraged to visit <https://dcoz.dc.gov/service/watch-live-virtual-zcbza-hearingsmeetings> to watch the live broadcast

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Web Site: www.dcoz.dc.gov

District of Columbia

CASE NO.21273

EXHIBIT NO.19

GOVERNMENT OF THE DISTRICT OF COLUMBIA
OFFICE OF ZONING
441 4th STREET, N.W. SUITE 200-S/210-S
WASHINGTON, D.C. 20001

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HARRY CASHWELL
4190 LIVINGSTON ROAD SE UNIT 103
WASHINGTON DC 20032

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WASHINGTON, D.C. 20001**

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MELANIA SCOTT
4190 LIVINGSTON ROAD SE UNIT 104
WASHINGTON DC 20032

NAME	ADDRESS	TELEGRAM	TELEPHONE	TELETYPE	TELEFAX
DR. J. R. BROWN	1000 15th Street, N.W. Washington, D.C. 20004	WASH 2-1234	202-467-5200	202-467-5200	202-467-5200
DR. J. R. BROWN	1000 15th Street, N.W. Washington, D.C. 20004	WASH 2-1234	202-467-5200	202-467-5200	202-467-5200
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卷四：民族学81271-民族学81279-885-4

Category	Sub-Category	Parameter	Value	Notes
System A	Processor	Core Clock	4.0 GHz	Max performance
		Memory Clock	3200 MHz	Optimized for memory bandwidth
System B	Processor	Core Clock	3.8 GHz	Balanced performance
		Memory Clock	3000 MHz	Optimized for memory bandwidth
System C	Processor	Core Clock	3.5 GHz	Low power consumption
		Memory Clock	2800 MHz	Optimized for memory bandwidth
System D	Processor	Core Clock	3.2 GHz	Low power consumption
		Memory Clock	2600 MHz	Optimized for memory bandwidth
System E	Processor	Core Clock	3.0 GHz	Low power consumption
		Memory Clock	2400 MHz	Optimized for memory bandwidth
System F	Processor	Core Clock	2.8 GHz	Low power consumption
		Memory Clock	2200 MHz	Optimized for memory bandwidth
System G	Processor	Core Clock	2.5 GHz	Low power consumption
		Memory Clock	2000 MHz	Optimized for memory bandwidth
System H	Processor	Core Clock	2.2 GHz	Low power consumption
		Memory Clock	1800 MHz	Optimized for memory bandwidth
System I	Processor	Core Clock	2.0 GHz	Low power consumption
		Memory Clock	1600 MHz	Optimized for memory bandwidth
System J	Processor	Core Clock	1.8 GHz	Low power consumption
		Memory Clock	1400 MHz	Optimized for memory bandwidth
System K	Processor	Core Clock	1.6 GHz	Low power consumption
		Memory Clock	1200 MHz	Optimized for memory bandwidth
System L	Processor	Core Clock	1.4 GHz	Low power consumption
		Memory Clock	1000 MHz	Optimized for memory bandwidth
System M	Processor	Core Clock	1.2 GHz	Low power consumption
		Memory Clock	800 MHz	Optimized for memory bandwidth
System N	Processor	Core Clock	1.0 GHz	Low power consumption
		Memory Clock	600 MHz	Optimized for memory bandwidth
System O	Processor	Core Clock	0.8 GHz	Low power consumption
		Memory Clock	400 MHz	Optimized for memory bandwidth
System P	Processor	Core Clock	0.6 GHz	Low power consumption
		Memory Clock	200 MHz	Optimized for memory bandwidth
System Q	Processor	Core Clock	0.4 GHz	Low power consumption
		Memory Clock	100 MHz	Optimized for memory bandwidth
System R	Processor	Core Clock	0.2 GHz	Low power consumption
		Memory Clock	50 MHz	Optimized for memory bandwidth
System S	Processor	Core Clock	0.1 GHz	Low power consumption
		Memory Clock	25 MHz	Optimized for memory bandwidth
System T	Processor	Core Clock	0.05 GHz	Low power consumption
		Memory Clock	12.5 MHz	Optimized for memory bandwidth
System U	Processor	Core Clock	0.025 GHz	Low power consumption
		Memory Clock	6.25 MHz	Optimized for memory bandwidth
System V	Processor	Core Clock	0.0125 GHz	Low power consumption
		Memory Clock	3.125 MHz	Optimized for memory bandwidth
System W	Processor	Core Clock	0.00625 GHz	Low power consumption
		Memory Clock	1.5625 MHz	Optimized for memory bandwidth
System X	Processor	Core Clock	0.003125 GHz	Low power consumption
		Memory Clock	0.78125 MHz	Optimized for memory bandwidth
System Y	Processor	Core Clock	0.0015625 GHz	Low power consumption
		Memory Clock	0.390625 MHz	Optimized for memory bandwidth
System Z	Processor	Core Clock	0.00078125 GHz	Low power consumption
		Memory Clock	0.1953125 MHz	Optimized for memory bandwidth

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BRIANNA BAMES
4196 LIVINGSTON ROAD SE UNIT 101
WASHINGTON DC 20032

ANK
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